A FULLY INTEGRATED 35 GHz MMIC RECEIVER WITH ON-CHIP LO

R.Ramachandran, C.Woo, M.Nijjar, D.Fisher

PACIFIC MONOLITHICS, INC
245 Santa Ana Court
Sunnyvale CA 94086-4512
408-732-8000

ABSTRACT

A fully integrated 35 GHz MMIC receiver chip has been designed, fabricated and tested. The chip contains a Low-Noise Amplifier (LNA), an active mixer, an IF amplifier, a local oscillator, and a buffer amplifier. The only external component required is the resonator. This feature was incorporated to accommodate both DRO and VCO implementations. Chip size is 54 x 80 mils (1.35 x 2 mm).

The MMIC chip exhibits a conversion gain of 17 $\pm$ 2 dB across the 33 to 37 GHz band with a peak gain of 19 dB at 34 GHz. IF bandwidth extends from 100 MHz to over 2 GHz and the noise figure (DSB) is 9 dB. When assembled with a varactor, the local oscillator has a tuning bandwidth of over 4 GHz. The entire chip draws 55 mA from a single +8 volt supply.

INTRODUCTION

Microwave frequency converters are essential parts of commercial communication systems, military radar, and electronic warfare systems. Traditional approaches using separate RF amplifiers, mixers, IF amplifiers, and oscillators are difficult and expensive to implement at mm-wave frequencies. Present research and development activities with MMIC devices offer promising results, however, several difficulties have been encountered regarding integration of all functions. Recent advances in multi-function MMIC converter chips in the 30 GHz band have been reported [1,2,3]. While these efforts combined the LNA, mixer, and IF amplifiers onto a single chip, an off-chip LO was still required. In addition, these devices required large amounts of real estate.

In this paper, we describe the design, fabrication and performance of a 35 GHz MMIC down converter that utilizes a drain-fed active mixer and an on-chip local oscillator to achieve high performance and small size (1.35 x 2 mm) with a single external component, the resonator.

DESIGN APPROACH

To achieve high performance in a 35 GHz receiver, the active device should be capable of high gain and low noise figure at mm-wave frequencies. Based on these requirements, a P-HEMT (Pseudomorphic HEMT) process was chosen. However, obtaining a suitable diode in this process is difficult. This forced the development of a drain-fed active mixer. Figure 1 shows the block diagram of the MMIC receiver. It consists of a Low Noise Amplifier (LNA), an active mixer, an IF amplifier, a Local Oscillator (LO), and a buffer amplifier.

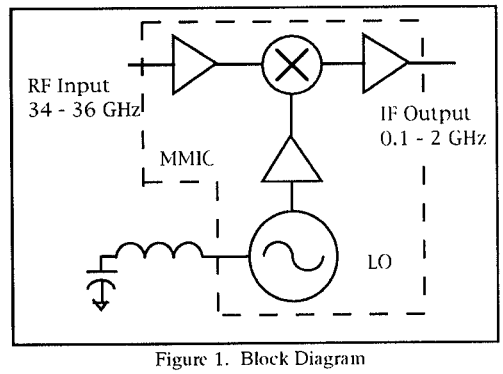

Figure 1. Block Diagram

The LNA is a single-stage design using a 75 micron wide P-HEMT with reactive matching at both the input and the output. A single stage design was chosen for simplicity and size. Optimization of gate width provided the best overall compromise between bandwidth and input match when using a single shunt tuning stub for noise figure. Simulations indicated that a gain of 6.5 dB was obtainable with 4 dB noise figure.

The mixer utilizes a 100 micron device in a drain-fed mixer configuration. The RF is fed into the gate while the LO is applied to the drain. The IF is extracted from the drain using a low-pass filter. The active mixer configuration results in low conversion loss and noise figure when operating at lower LO drive levels. The most important benefit is eliminating the need for high quality diodes (which are incompatible with P-HEMT MMIC processes). Non-linear simulations, with an internally developed model, indicated that a conversion loss of 0 dB is obtainable with an LO drive level of +5 dBm.

The local oscillator utilizes a 120 micron device with a feedback capacitor in the source to generate negative resistance. The drain is terminated in a low impedance to maximize negative R. The oscillator also includes a single stage buffer amplifier that provides isolation from the load and increased output power. Current consumption was minimized by connecting the LO and the buffer amplifier in a totem-pole configuration.

The IF amplifier is a single-stage feedback design using a 300 micron interdigitated FET with an active load. The active load eliminates the need for a large on-chip inductor which would waste GaAs real estate. Additionally, the active load drops the + 8 volts supply to + 4 volts for the IF amplifier FET. Simulated gain was 16 dB over the 0.1 to 2 GHz band.

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The high level of integration of this chip required accurate simulation of each component and their related interactions. A top level non-linear simulation of the full converter was required to confirm that design goals were obtainable. Careful attention to mutual coupling was necessary to maintain the compact chip size.

PERFORMANCE OF COMPONENTS AND RECEIVER MMIC

Figure 2 is a photograph of the fabricated chip. Figure 3 is a plot of measured gain and input return loss of the LNA. The measured LNA peak gain was 8 dB (at 35 GHz) with a minimum gain of 6 dB over the full 33 to 37 GHz band. Measured noise figure was 4.5 dB at 34 GHz (see Figure 4). These results are in good agreement with simulations (6.5 dB gain and 4 dB Noise Figure).

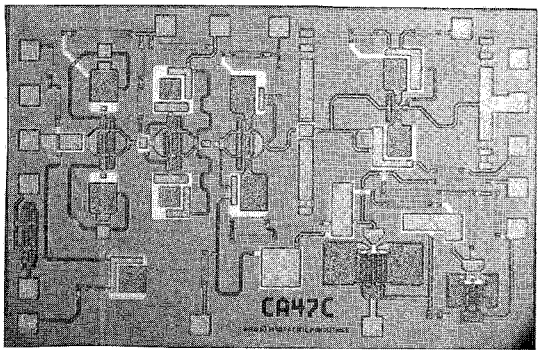

Figure 2. Chip Photograph

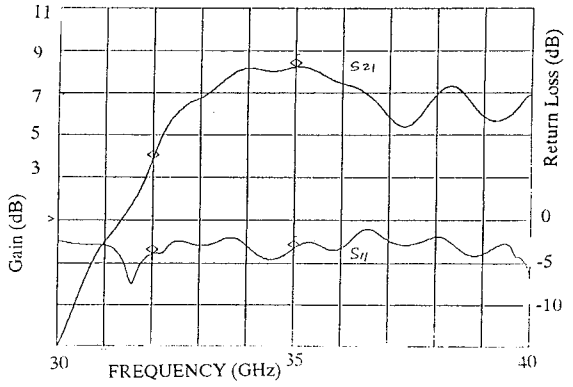

Figure 3. LNA Gain & Return Loss

The mixer IF bandwidth covered 0.1 to 2 GHz with a 4 dB conversion loss at 35 GHz (see Figure 5). The LO was held at 34 GHz and + 5 dBm while the RF was swept from 34.1 to 36 GHz at -7 dBm input power. The higher than expected conversion loss was traced to high device C_{gd}.

The local oscillator circuit was tested using a dielectric puck as the resonator and results are shown in Figure 6. The output was monitored using a spectrum analyzer and harmonic mixer. The measured phase noise was -85 dBc/Hz at a 100 kHz offset, with an output power of +5 dBm.

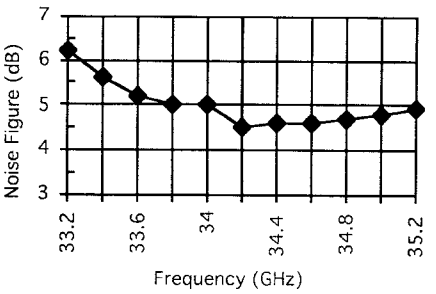

Figure 4. LNA Noise Figure

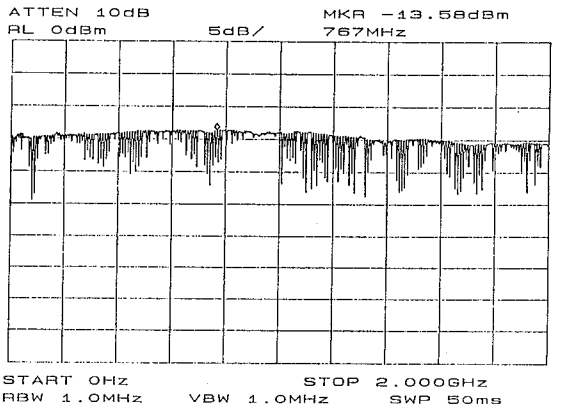

Figure 5. Mixer IF Output

The IF amplifier measured gain was 13 dB in the 0.1 to 2 GHz frequency range with a 10 dB noise figure at 1 GHz. Excellent bandwidth was obtained with gain at 5 GHz exceeding 10 dB (see Figure 7). The higher noise figure and lower gain (than anticipated from simulations) were caused by overetching of the larger size devices used in the IF amp. A processing problem occurred whereby interdigitated FETs with large periphery (300 um) etched at a faster rate than the smaller FETs. This caused high parasitic resistance, low g_m, and required 0.7 volts gate-to-source for operation. The equivalent circuit models of the smaller devices (used for the LNA, mixer, oscillator and buffer amplifier) were closer to foundry specifications.

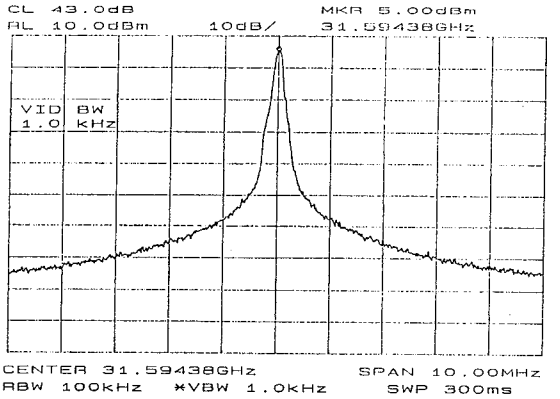

Figure 6. Output Spectrum of DRO

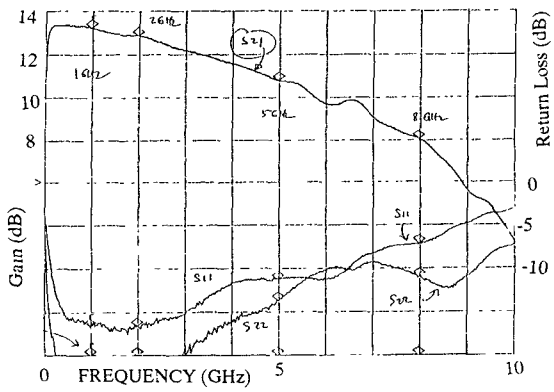

Figure 7. IF Amplifier Performance

After thorough characterization of the individual components, the complete receiver MMIC was assembled for testing using both a DRO and a VCO implementation of the on-chip local oscillator. Figure 8 shows the measured conversion gain with the RF input swept from 33 to 37 GHz when coupling a dielectric resonator to the on-chip oscillator. The gain over the full 33 to 37 GHz band is greater than 15 dB with a 19 dB peak at 34 GHz. A 9.2 dB receiver noise figure was measured and by optimizing the LNA and mixer bias, a minimum noise figure of 8.5 dB could be obtained.

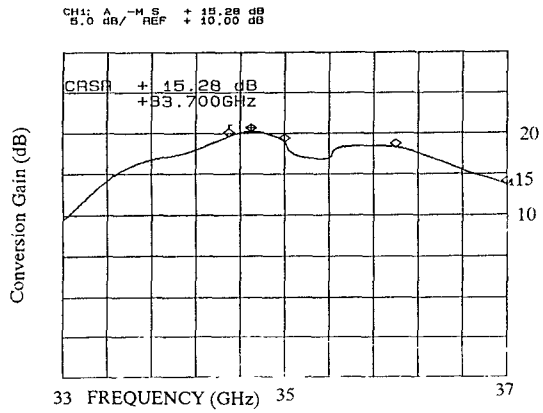

Figure 8. Conversion Gain of MMIC with on-chip DRO

The MMIC receiver was also assembled with a 0.5 pF GaAs varactor connected to the on-chip oscillator. The VCO demonstrated 4 GHz of tuning bandwidth and could be tuned from 34 to 38 GHz. Figure 9 shows the conversion gain of the receiver measured with the VCO set to 35 GHz and the RF input swept from 33 to 37 GHz. A peak conversion gain of 17.4 dB was obtained at 34.5 GHz with minimum noise figure of 9.5 dB at 35.1 GHz.

The overall performance of the MMIC receiver and its components is summarized in the following table:

COMPONENT	MEASURED
RF amp	8 dB gain
	4.5 dB NF
Mixer	4 dB conversion loss
IF amp	13 dB gain
	10 dB NF
Oscillator	8 dBm power out
MMIC Receiver	17 dB gain
	9.5 dB NF
Bias	55 mA @ 8 V

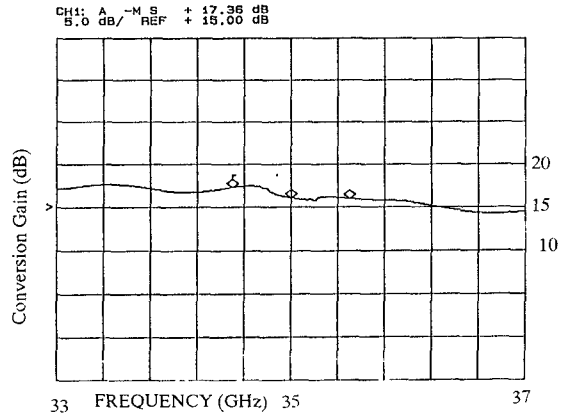

Figure 9. Conversion Gain of MMIC with on-chip VCO

SUMMARY

A 35 GHz MMIC receiver incorporating an on-chip local oscillator and an active drain-fed mixer has been designed, fabricated and tested. The high level of integration required a dense layout to achieve the smallest reported chip size (54 X 80 mils) for this level of functionality. Additionally, very good performance was demonstrated in a receiver assembly requiring only one external component.

ACKNOWLEDGMENTS

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